ABSTRACT

A high-bandwidth data transfer apparatus that is suitable for modular and scalable processing systems is disclosed. In one embodiment, the data transfer apparatus includes a local bus between each of several processing devices and associated memory modules. The local busses are each coupled to a cross-bus through a bus bridge that consists of multiplexers to steer address and data signals from a local bus along the cross-bus to another local bus. The multiplexer structure of the bridges allows the cross-bus to be dynamically divided into segments in any suitable manner to support multiple concurrent links over the cross-bus. A controller is provided to set the multiplexers in accordance with transfer requests that it receives from the various processing devices. The transfer requests may be of various types such as: single transfer, block transfer, and/or message transfer. The controller may include a request queue for each type of transfer request. The controller may also include a direct memory access controller (DMA) for facilitating the block transfers, and may further include an interrupt controller for notifying the processing devices of various events such as: receipt of a message transfer request, completion of block transfer, and/or memory protection violation. The data transfer apparatus may include a processor interface port for each processor. The ports may be configured to enforce programmable memory protection settings. When applied to multimedia systems with a microcontroller, one or more digital signal processors, and one or more hardware accelerators, this data transfer apparatus is expected to provide a substantial increase in processing capabilities.